情報電子工学科　学会発表

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学会名	The 4th International Conference on Fuzzy Systems and Data Mining (FSDM 2018)
演題名	Foundations of Hierarchical Model Checking: Logics, Translations, and Examples
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内容	Hierarchical model checking is a model-checking paradigm that can appropriately verify systems with hierarchical information and structures. In this study, logics and translations for hierarchical model checking are developed on the basis of linear-time temporal logic (LTL), computation-tree logic (CTL), and full computation-tree logic (CTL*). A sequential linear-time temporal logic (sLTL), a sequential computation-tree logic (sCTL), and a sequential full computation-tree logic (sCTL*), which can suitably represent hierarchical information and structures, are developed by extending LTL, CTL, and CTL*, respectively. Translations from sLTL, sCTL, and sCTL* into LTL, CTL, and CTL*, respectively, are defined, and theorems for embedding sLTL, sCTL, and sCTL* into LTL, CTL, and CTL*, respectively, are proved using these translations. These embedding theorems allow us to reuse the standard LTL-, CTL-, and CTL*-based model-checking algorithms to verify hierarchical systems that are modeled and specified by sLTL, sCTL, and sCTL*. Some illustrative examples of hierarchical model checking are also presented on the basis of the proposed logics and translations.